WHAT IS CLAIMED IS:

Claim 1. A hand held vibration data collector and analyzer system for collecting, analyzing, and storing vibration data that is produced by and collected from a predetermined series of machines and for transferring data to a computer, comprising:

a vibration transducer for sensing vibration that is produced by the machines and for producing an analog vibration signal corresponding to the vibration;

a housing dimensioned and configured for being hand held;

a conditioning circuit mounted in said housing:

(a) for receiving and conditioning the analog vibration signal from the vibration transducer to produce a conditioned analog signal;

(b) including a fixed frequency analog anti-aliasing filter having a fixed upper cutoff frequency set at a desired frequency equal to the maximum vibration frequency of interest for producing the conditioned analog signal having a desired frequency range;

(c) including amplifiers for producing the conditioned analog signal at a desired amplitude;

(d) including an analog to digital converter (ADC) for receiving and sampling the conditioned analog signal to produce a digital signal;

a data processor mounted in said housing for processing the digital signal to produce desired digital data, said data processor including:

a transformer for selectively operating on the digital signal, performing a Fast Fourier Transform, and producing a frequency spectrum from the digital signal;

a selector for selecting and producing select data for storage from at least one of the digital signal and the frequency spectrum;

a keyboard mounted in said housing interfaced with said data processor for inputting commands and data to said data processor;

a display mounted in said housing interfaced with said data processor for displaying information to the user;

memory interfaced with the data processor for storing information including the select data; and

means for transferring information that is stored in said memory to the computer.

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Claim 2. The system of Claim 1 wherein said data processor further comprises a digital filter and decimator for optionally reducing the sample rate and frequency content of the digital signal to produce a modified digital signal.

Claim 3. The system of Claim 1 wherein said conditioning circuit further comprises:

a third order sigma-delta modulator having three cascaded sigma-delta loops and having a transfer function substantially of: $Y(z) = X(z) + (1-Z^{-1})^{-3}Q^3(Z)$ where Q^3 is the quantization noise from the third order sigma-delta loop, said modulator receiving the conditioned analog signal and producing a digital modulator signal;

a comb filter for digitally low-pass filtering and decimating the digital modulator signal from said modulator to produce a comb signal; and

a FIR filter for digitally low-pass filtering and decimating the comb signal to produce the digital signal for said data processor.

Claim 4. The system of Claim 1 wherein:

said conditioning circuit further comprises hardware for receiving and sampling the conditioned analog signal at a sample frequency that is substantially greater than a maximum frequency of interest to produce a digital signal, and further for digitally low-pass filtering and digitally decimating the digital signal to produce a conditioned digital signal having a reduced sample rate as compared to the digital signal and a predetermined upper cutoff frequency; and

said data processor further comprising a digital low- pass filter and decimator for optionally and selectively reducing the sample rate and frequency content of the conditioned digital signal to produce a modified conditioned digital signal.

Claim 5. The system of Claim 1 wherein said data processor further comprises a zoom processor for operating on the digital signal to produce a zoom digital signal having a frequency range that is reduced compared to the frequency range of the digital signal.

Claim 6. The system of Claim 1 wherein said data processor further comprises:

a zoom processor for operating on the digital signal to produce a zoom digital signal having a frequency range that is

reduced compared to the frequency range of the digital signal; and

a transformer for selectively operating on the zoom digital signal, performing a Fast Fourier Transform, and producing a zoom frequency spectrum from the zoom digital signal.

Claim 7. The system of Claim 1 wherein said data processor further comprises a zoom processor for operating on the digital signal by frequency shifting the digital signal and low-pass filtering the frequency shifted digital signal to produce a zoom digital signal corresponding to a selected band of frequencies in the digital signal ranging from a selected upper frequency to a selected lower frequency, both of which are greater than one hertz.

Claim 8. The system of Claim 1 wherein said data processor further comprises a zoom processor for operating on the digital signal by multiplying the digital signal by a function to frequency shift the digital signal and low-pass filtering the frequency shifted digital signal to produce a zoom digital signal corresponding to a selected band of frequencies in the digital signal ranging from a selected upper frequency to a selected lower frequency, which is greater than one hertz.

Claim 9. The system of Claim 1 wherein said data processor further comprises a zoom processor for producing a zoom digital signal corresponding to a frequency band in the digital signal, said frequency band having an upper frequency, a lower frequency and a center frequency that is centered between the upper and lower frequencies of the band, said zoom processor for frequency shifting the digital signal to shift the center frequency to zero and low-pass filtering the frequency shifted digital signal to produce a zoom digital signal in which the lower and upper frequencies in the zoom digital signal correspond to the lower and upper frequencies in said band, respectively.

Claim 10. The system of Claim 1 wherein said data processor further comprises:

a zoom processor for operating on the digital signal by frequency shifting the digital signal and low-pass filtering the frequency shifted digital signal to produce a zoom digital signal corresponding to a selected band of frequencies in the digital signal ranging from a selected upper frequency to a selected lower frequency and having a center frequency;

said zoom processor multiplying the digital signal by a function equal to $e^{2\pi i(f0)/(fs)}$, where f0 equals the center frequency of the selected band and fs equals the sample rate of the digital signal, to frequency shift the digital signal such that the center frequency is shifted to zero;

said zoom processor low-pass filtering the frequency shifted digital signal to produce a zoom digital signal in which the lower and upper frequencies in the zoom digital signal correspond to the lower and upper frequencies in said band, respectively.

Claim 11. The system of Claim 10 wherein said data processor further comprises a transformer for Fast Fourier Transforming the frequency shifted digital signal to produce a zoom frequency spectrum corresponding to the selected frequency band of the digital signal.

Claim 13. The system of Claim 1 wherein said data processor further comprises:

a digital signal processor (DSP) connected to receive and for operating on the digital signal independently performing Fast Fourier Transforms on the digital signal to produce a frequency spectrum; and

a central processing unit (CPU) for controlling the operation of the system including the operation of the DSP, said DSP performing the Fast Fourier Transform independently of the CPU.

Claim 14. The system of Claim 1 wherein said data processor further comprises:

a DSP connected to receive and operate on the digital signal independently performing Fast Fourier Transforms on the digital signal to produce a frequency spectrum, performing a rastering operation on the spectrum to generate a graphical representation of the frequency spectrum, and transferring the graphical representation to said memory;

a CPU for controlling the operation of the system including the issuing of commands to said DSP causing said DSP to perform operations independently of the CPU; and

a direct memory access (DMA) for transferring data directly to said memory without interrupting the CPU, said DMA transferring data including the frequency spectrum and the graphical representation from said DSP to said memory.

Claim 15. The system of Claim 1 wherein said data processor

comprises:

a DSP serially connected to receive the digital signal from said analog to digital converter;

a CPU for generating commands to control the operation of the system including the DSP;

said DSP for operating on and analyzing the digital signal independently of the CPU to produce an analyzed digital signal representing selected properties of the digital signal and for transmitting the analyzed digital signal to said memory independently of the CPU; and

said CPU for transmitting commands to said DSP to select the operations and analysis that is performed on the digital signal by the DSP.

Claim 15. The system of Claim 14 wherein said DSP in response to commands from said CPU performs a Fast Fourier Transform independently of said CPU on the digital signal to produce a frequency spectrum representative of the frequency content of the digital signal.

Claim 16. The system of Claim 14 wherein said DSP in response to commands from said CPU performs a zoom operation independently of said CPU on the digital signal to produce a zoom digital signal representative of a selected frequency band in the digital signal.

Claim 17. The system of Claim 14 wherein said DSP in response to commands from said CPU performs a low-pass filtering and decimation operation on the digital signal independently of said CPU to produce a filtered digital signal having a reduced sample rate as compared to the digital signal and being representative of a portion of the digital signal having a frequency below a selected upper frequency.

Claim 18. The system of Claim 14 wherein said DSP in response to commands from said CPU performs:

a low-pass filtering and decimation operation on the digital signal independently of said CPU to produce a filtered digital signal having a reduced sample rate as compared to the digital signal and being representative of a portion of the digital signal having a frequency below a selected upper frequency;

a zoom operation independently of said CPU signal to produce a zoom digital signal representative of a selected frequency band in the digital signal; and

a Fast Fourier transform independently of said CPU to produce a frequency spectrum representative of a frequency content of the digital signal.

Claim 10. The system of Claim 1 wherein said memory further comprises:

a memory card for storing data in a card format:

a plug system for connecting and disconnecting said memory card to and from the system;

a random access memory (RAM) interfaced with said data processor for storing data; and

a RAM formatter for controlling the flow of data to and from said RAM and configuring said RAM as a pseudo-card so that said RAM in conjunction with said RAM formatter functions substantially identically as said memory card, receiving and transmitting data in card format.

Claim 30. A hand held data collector and analyzer system for collecting, analyzing, and storing data and for transferring data to a computer, comprising:

a main transducer for sensing analog data and for producing a main analog signal corresponding to the analog data;

an optional transducer for sensing analog data and for producing an optional analog signal corresponding to the analog data;

a housing adapted to be hand held;

a main conditioning circuit mounted in said housing:

(a) for receiving and conditioning the main analog signal from said main transducer to produce a conditioned main analog signal;

(b) including a fixed frequency main analog anti-aliasing filter having an upper cutoff frequency for producing the conditioned main analog signal having a desired frequency range;

(c) including amplifiers for producing the conditioned main analog signal at a desired amplitude;

(d) a main analog to digital converter (ADC) for receiving and sampling the conditioned main analog signal to produce a main digital signal; and

(e) a main microprocessor controller for controlling said main conditioning circuit;

an optional conditioning circuit mounted in said housing:

(a) for receiving and conditioning the optional analog signal from said optional transducer to produce a conditioned optional analog signal;

(b) including a fixed frequency optional analog anti-aliasing filter having an upper cutoff frequency for producing the conditioned optional analog signal having a desired frequency range;

(c) including amplifiers for producing the conditioned optional analog signal at a desired amplitude; and

(d) an optional ADC for receiving and sampling the conditioned optional analog signal to produce an optional digital signal;

a main digital signal processor (DSP) mounted in said housing connected to serially receive the main digital signal and for selectively operating on the main digital signal, performing a Fast Fourier Transform, and producing a main frequency spectrum;

an optional DSP mounted in said housing connected to said optional conditioning circuit for serially receiving the optional digital signal and for selectively operating on the optional digital signal, performing a Fast Fourier Transform, and producing a frequency spectrum from the optional digital signal;

a central processing unit (CPU) mounted in said housing for controlling the overall operation of the system including the issuing of commands to said optional DSP and said main microprocessor controller;

a main interface connecting said CPU to said main DSP and said main microprocessor controller;

an optional interface for connecting said CPU to said optional DSP;

said main microprocessor controller for controlling said main analog input conditioning circuitry and said main ADC in response to commands from said CPU;

said optional DSP for controlling said optional analog input conditioning circuitry and said optional ADC in response to commands from said CPU;

a keyboard mounted in said housing for inputting commands and data to said CPU;

a display mounted in said housing for displaying information to the user in response to commands of said CPU;

memory interfaced with said CPU and said main and optional DSP's for storing information including the select data; and

means for transferring information stored in said memory to the computer.

Claim 31. The system of Claim 30 wherein:

said main and optional conditioning circuits further comprise main and optional hardware for receiving and sampling the conditioned main analog signal and the conditioned optional analog signal, respectively, at sample frequencies that are substantially greater than maximum frequencies of interest to produce main and optional digital signals, and further for digitally low-pass filtering and digitally decimating the main and optional digital signals, respectively, to produce main and optional conditioned digital signals having reduced sample rates as compared to the main and optional digital signals, respectively, and having predetermined upper cutoff frequencies; and

said main and optional DSP's further comprising main and optional digital low-pass filter and decimators, respectively, for optionally and selectively reducing the sample rates and frequency content of the main and optional conditioned digital signals to produce main and optional modified conditioned digital signals.

Claim 32. The system of Claim 30 wherein said main DSP and said optional DSP, in response to commands from said CPU, performs:

a low-pass filtering and decimation operation independently of said CPU to produce main and optional filtered digital signals, respectively, having reduced sample rates as compared to the main and optional digital signals, respectively, and being representative of a portion of the main and optional digital signals;

a zoom operation independently of said CPU to produce main and optional zoom digital signals, respectively, representative of selected frequency bands in the main and optional digital signals; and

a Fast Fourier Transform independently of said CPU to produce frequency spectrums representative of a frequency content of the main and optional digital signals.

Claim 33. The system of Claim 30 wherein said optional

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conditioning circuit further comprises:

a separate optional circuit board; and

plug means for selectively connecting and disconnecting said optional circuit board to and from the system.

Claim 24. The system of Claim 20 wherein:

said main and optional DSP's operate on and analyze the main and optional digital signals independently of the CPU to produce main and optional analyzed digital signals representing selected properties of the main and optional digital signals, and transmit the analyzed digital signals to said memory independently of the CPU; and

said CPU includes a direct memory access (DMA) interconnected with said main and optional DSP's and with said memory for transferring data from said main and optional DSP's to said memory without interrupting said CPU.

Claim 25. A hand held vibration monitoring system for collecting, analyzing, and storing vibration data that is produced by and collected from a predetermined series of machines and for transferring data to a computer, comprising:

a vibration transducer for sensing vibration that is produced by the machines and for producing an analog vibration signal corresponding to the vibration;

a conditioning circuit:

(a) for receiving and conditioning the analog vibration signal from the vibration transducer to produce a conditioned analog signal;

(b) including hardware for receiving and sampling the conditioned analog signal at a sample frequency to produce a digital signal, and further for digitally low-pass filtering and digitally decimating the digital signal to produce a conditioned digital signal having a reduced sample rate as compared to the digital signal and a predetermined upper cutoff frequency;

a data processor for digitally processing and analyzing the conditioned digital signal to produce select data for storage;

a keyboard interfaced with said data processor for inputting commands and data to said data processor;

a display interfaced with said data processor for displaying information to the user;

memory interfaced with said data processor for storing data including the select data; and

means for transferring information stored in said memory to the computer.

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Claim 26. The system of Claim 25 wherein said data processor further ~~comprises~~ a digital low-pass filter and decimator for optionally and selectively reducing the sample rate and frequency content of the conditioned digital signal to ~~produce a modified conditioned digital signal.~~

Claim 27. 30 The system of Claim 25 35 wherein said data processor further comprises an analyzer for digitally analyzing the conditioned digital signal as to frequency content to produce frequency spectrum data corresponding to at least a portion of the conditioned digital signal.

Claim 28. 38 A hand held data collector and analyzer system for collecting, analyzing, and storing data and for transferring data to a computer, comprising:

a transducer for sensing analog data and for producing an analog signal corresponding to the analog data;

a conditioning circuit:

(a) for receiving and conditioning the analog signal from the transducer to produce a conditioned analog signal;

(b) including hardware for receiving and sampling the conditioned analog signal at a sample frequency to produce a digital signal, and further for digitally low-pass filtering and digitally decimating the digital signal to produce a conditioned digital signal having a reduced sample rate as compared to the digital signal and a predetermined upper cutoff frequency;

a data processor for processing the conditioned digital signal to produce desired digital data, said data processor comprising:

a digital low-pass filter and decimator for optionally and selectively reducing the sample rate and frequency content of the conditioned digital signal to produce a modified conditioned digital signal,

a zoom processor for selectively and optionally operating on the conditioned digital signal and the modified conditioned digital signal to produce zoom digital signals having a frequency range that is reduced compared to the frequency range of the conditioned digital signal or the modified conditioned digital signal, respectively, and

said digital low-pass filter and decimator of the data

processor for optionally and selectively reducing the sample rate and frequency content of the zoom digital signal to produce a modified zoom digital signal,

a transformer for selectively and optionally operating on the conditioned digital signal, the modified conditioned digital signal, the zoom digital signal, and the modified zoom digital signal, performing a Fast Fourier Transform, and selectively producing frequency spectrums;

a selector for selecting and producing select data for storage from the conditioned digital signal, the modified conditioned digital signal, the zoom digital signals, the modified zoom digital signals, and the frequency spectrums;

a digital control interface connected between said data processor and said digital conditioner;

said data processor for transmitting control signals through said digital control interface for selecting the upper cutoff frequency and output sample rate for the low-pass filtering and the decimating of said hardware, and for selecting the upper cutoff frequency and the output sample rate for the digital filter and decimator in the data processor;

a keyboard interfaced with said data processor for inputting commands and data to said data processor;

a display interfaced with said data processor for displaying information to the user, said information including the conditioned digital signal, the modified conditioned digital signal, the zoom digital signal, and the frequency spectrums;

memory interfaced with the data processor for storing information including the select data; and

means for transferring information stored in said memory to the computer.

Claim 39. A hand held vibration monitoring system for collecting, analyzing, and storing vibration data that is produced by and collected from a predetermined series of machines and for transferring data to a computer, comprising:

a transducer for sensing vibration that is produced by the machines and for producing an analog vibration signal corresponding to the vibration;

a conditioning circuit

(a) for receiving and conditioning the analog vibration signal from the vibration transducer to produce a conditioned

analog signal;

(b) including an anti-aliasing filter having an upper cutoff frequency set at a desired frequency for producing the conditioned analog signal having a desired frequency content;

(c) including amplifiers for producing the conditioned analog signal at a desired amplitude;

(d) including a first analog to digital converter (ADC) for receiving and sampling the conditioned analog signal at a relatively high sample rate to produce a first digital signal; and

(e) a second ADC for receiving and sampling the conditioned analog signal at a relatively low sample rate to produce a second digital signal, said second ADC being more accurate and stable in the conversion of substantially constant amplitude signals and low frequency signals in the range of about one hertz than said first analog to digital converters;

a data processor for receiving and digitally processing the first and second digital signals to produce desired digital data, and for selecting and producing select data for storage from the digital signals or the desired data;

a keyboard interfaced with said data processor for inputting commands and data to said data processor;

a display interfaced with said data processor for displaying information to the user;

memory interfaced with the data processor for storing information including the select data; and

means for transferring information that is stored in said memory to the computer.

Claim 40. The apparatus of Claim 39 wherein said first ADC operates with a sampling frequency of about 3.276 megahertz to 0.3276 megahertz and said second ADC operates with a sampling frequency of about 20 hertz.

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